

INTL9548 Product Brief

1. Description

Serving as an octal bidirectional translating switch, the INTL9548 is controlled through the I2C-bus. The SCL/SDA upstream pair is distributed to eight downstream pairs, or channels. Users can choose individual SCx/SDx channel or combination of channels based on programmable control register. An active LOW reset input is provided so that the INTL9548 can recover if one of the downstream I2C-buses gets stuck in a LOW state. Pulling the $\overline{\text{RESET}}$ pin LOW resets the I2C-bus state machine. This will deselect all the channels, similar to the internal Power-On Reset (POR) function.

The switches are designed with pass gates so that the VDD pin can restrict the maximum high voltage passed by the INTL9548, different bus voltages can be used on each pair, and 1.8V or 2.5V or 3.3V parts can communicate with 5V parts without any additional protection. External pull-up resistors are used to adjust the bus up to the desired voltage level for each channel. Each I/O pin is 5V tolerant.

2. Features

- 1-of-8 bidirectional translating switches
- I2C-bus interface logic; compatible with SMBus standards
- Active LOW reset input
- 3 address pins allowing up to 8 devices on the I2C-bus
- Channel selection via I2C-bus, in any combination
- Power-up with all switch channels deselected
- Low Ron switches
- Allows voltage level translation between 1.8V, 2.5V, 3.3V and 5V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 1.65-5.5V
- 5V tolerant Inputs
- 0Hz to 400kHz clock frequency
- ESD protection exceeds 2000V HBM per JESD22-A114 and 1000VCDM per JESD22-C101
- Latch-up testing is carried out according to JEDEC Standard JESD78 at a current over 150mA
- Operating Temperature=-40°C to 85°C
- Available package:
TSSOP-24(4.40mm X 7.80mm)

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3. Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I2C Slave Address Conflicts

4. Functional Diagram

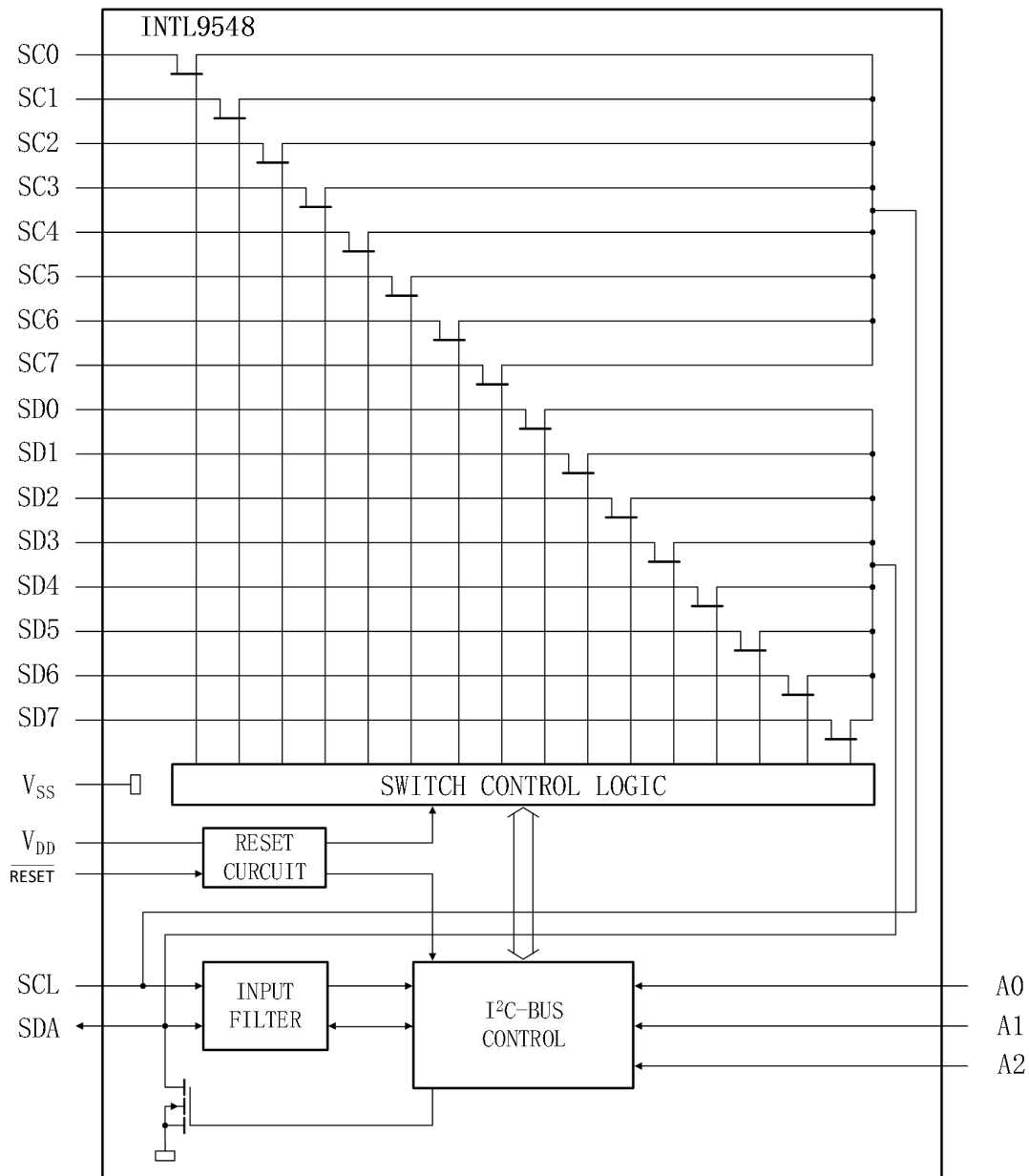


Figure 1 Functional Diagram